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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,253	08/27/2003	Yuan-Jen Chao	4459-0149P	5216

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EXAMINER	
CARPIO, IVAN HERNAN	
ART UNIT	**PAPER NUMBER**
2841	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/24/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/648,253	CHAO, YUAN-JEN	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. Examiner notes that the final rejection of 12/15/2005 is hereby withdrawn in light of the arguments in the appeal brief filed 08/14/2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3-5,8-14,16,19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Feldman (US 6097857).

With respect to claim 1 Feldman teaches a multi-chip integrated module (Fig. 5 and Fig. 6), comprising: a transparent substrate (Fig. 6, element 17'), which has a circuit layer formed on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection (Fig. 6, elements 47) and a plurality of electrical pads (Fig. 6, elements 20'); at least two chips (Fig. 5, elements 13' and 15'), which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system; and a circuit substrate (Fig. 6, element 45), which attaches to the transparent substrate, and at least comprises

a circuit layer (Fig. 6, element 40') of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate.

With respect to claim 3 and with all the limitations of claim 1, Feldman teaches that a plurality of bumps (Fig. 6, element 24') are formed on the electrical pads of the transparent substrate, respectively, for electrically connecting the electrical pads and the circuit layer of the circuit substrate.

With respect to claim 4 and with all the limitations of claim 1, Feldman teaches that a plurality of bumps are formed on a part of the circuit for electrical inter-connection, and the chips electrically connect to the bumps by way of a flip-chip bonding (Fig. 6, elements 24').

With respect to claim 5 and with all the limitations of claims 3 or 4, Feldman teaches that the bumps are solder bumps (Fig. 6, element 24').

With respect to claim 8 and with all the limitations of claim 1, Feldman teaches that the circuit substrate has a hollow portion, and when the circuit substrate attaches to the transparent substrate, the chips are positioned in the hollow portion of the circuit substrate (Fig. 6, the hollow space that chips 13' and 15' are located in).

With respect to claim 9 and with all the limitations of claim 8, Feldman teaches a heat dissipation element (Fig. 5, element 45 and 11') is formed on the backside of at least one of the chips.

With respect to claim 10 and with all the limitations of claim 1, Feldman teaches that the circuit substrate is a printed circuit substrate (Fig. 6, element 45).

With respect to claim 11 and with all the limitations of claim 1, Feldman teaches a passive component (Fig. 6, element 25'), which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

With respect to claim 12 and with all the limitations of claim 1, Feldman teaches an active component (Fig. 6, element 13'), which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

With respect to claim 13 Feldman teaches a multi-chip integrated module, comprising: a transparent substrate (Fig. 6, element 17'), which has a circuit layer formed on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection (Fig. 6, element 47), and a plurality of bumps (Fig. 6, element 24') are formed on a part of the circuit for electrical inter-connection; and at least two chips (Fig. 5, elements 13' and 15'), which electrically connect to the bumps of the circuit for electrical inter-connection by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system.

With respect to claim 14 and with all the limitations of claim 13, Feldman teaches that the circuit layer of the transparent substrate further comprises a plurality of electrical pads (Fig. 6, elements 20') for electrical external-connection, and a plurality of bumps (Fig. 6, element 24') are formed on the electrical pads, respectively.

With respect to claim 16 and with all the limitations of claim 13 or 14, Feldman teaches the bumps are solder bumps (Fig. 6, element 24').

Claims 19 and 20 are rejected with the same logic as claims 11 and 12.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldman in view of Okano (US 5679928).

With respect to claims 2 and 15, Feldman teaches all of the limitations except that the transparent substrate is a glass substrate. Glass substrates are well known in the art, there are many different materials used for substrates in this art and the choice of material is dependant on specific properties needed such as the thermal expansion coefficient. Okano teaches a glass substrate in a multi-chip integrated module (Fig. 1a, element 32). It would have been obvious to one of ordinary skill in the art at the time of the invention to use a glass substrate, as taught by Okano, for the transparent substrate taught by Feldman, for the purpose of fulfilling necessary properties specific to the intended use. Furthermore it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Claims 6,7,17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldman in view of Lin (US 5018005).

With respect to claims 6, 7, 17 and 18 Feldman teaches all of the limitations except that the bumps are gold bumps (as in claims 1 and 17) or copper bumps (as in claims 7 and 18). Gold bumps and copper bumps are well known in the art, the particular material for bumps is dependant on specific properties needed such as the coefficient of electrically conductivity. Lin teaches the use of gold bumps (column 5, lines 63-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to use gold bumps, as taught by Lin, for the bumps taught by Feldman, for the purpose of fulfilling necessary properties specific to the intended use. Furthermore it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on T-F 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IC

TUAN T. DINH
PRIMARY EXAMINER